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(54) Abstract Title
A synchronising circuit for a PBX for synchronising a PCM clock signal with basic rate ISDN signals

(57) A communications circuit (1) of a PBX comprises a control circuit (3) for controlling the circuit (1) and an interface circuit (4) which operates under the control of the control circuit (3) for receiving eight ISDN lines on inputs (1) to (8) of the interface circuit (4). Integrated circuit chips (5) are provided, one for each ISDN line, each one outputs a line synchronous clock signal which is derived from the basic rate ISDN network signal on the corresponding ISDN line. A synchronising circuit (2) comprises a digital phase locked loop circuit (IC 24) for providing synchronised PCM clock signals one of which is applied to an input (1) of a digital switch matrix (6) for clocking ISDN signals through the digital switch matrix (6). The phase locked loop circuit (IC 24) outputs the synchronised PCM clock signal which is divided in a digital counter (IC 23), (IC 30) and (IC 31) to appropriate frequencies. The synchronised PCM clock signal is fed back to the digital phase locked loop circuit (IC 24) where it is compared with one of the line synchronous clock signals which is selected by a multiplexer (IC 26). The two signals are compared in the digital phase locked loop circuit (IC 24) and single pulses at the same frequency as the synchronised PCM clock signal are added to or deleted from the synchronised PCM clock signal to push the signal into phase and phase lock the signal with the selected line synchronous clock signal.

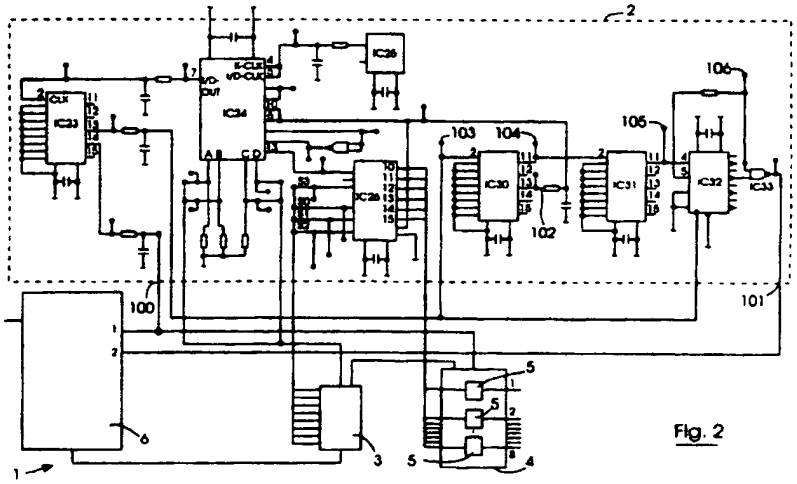

Fig. 2

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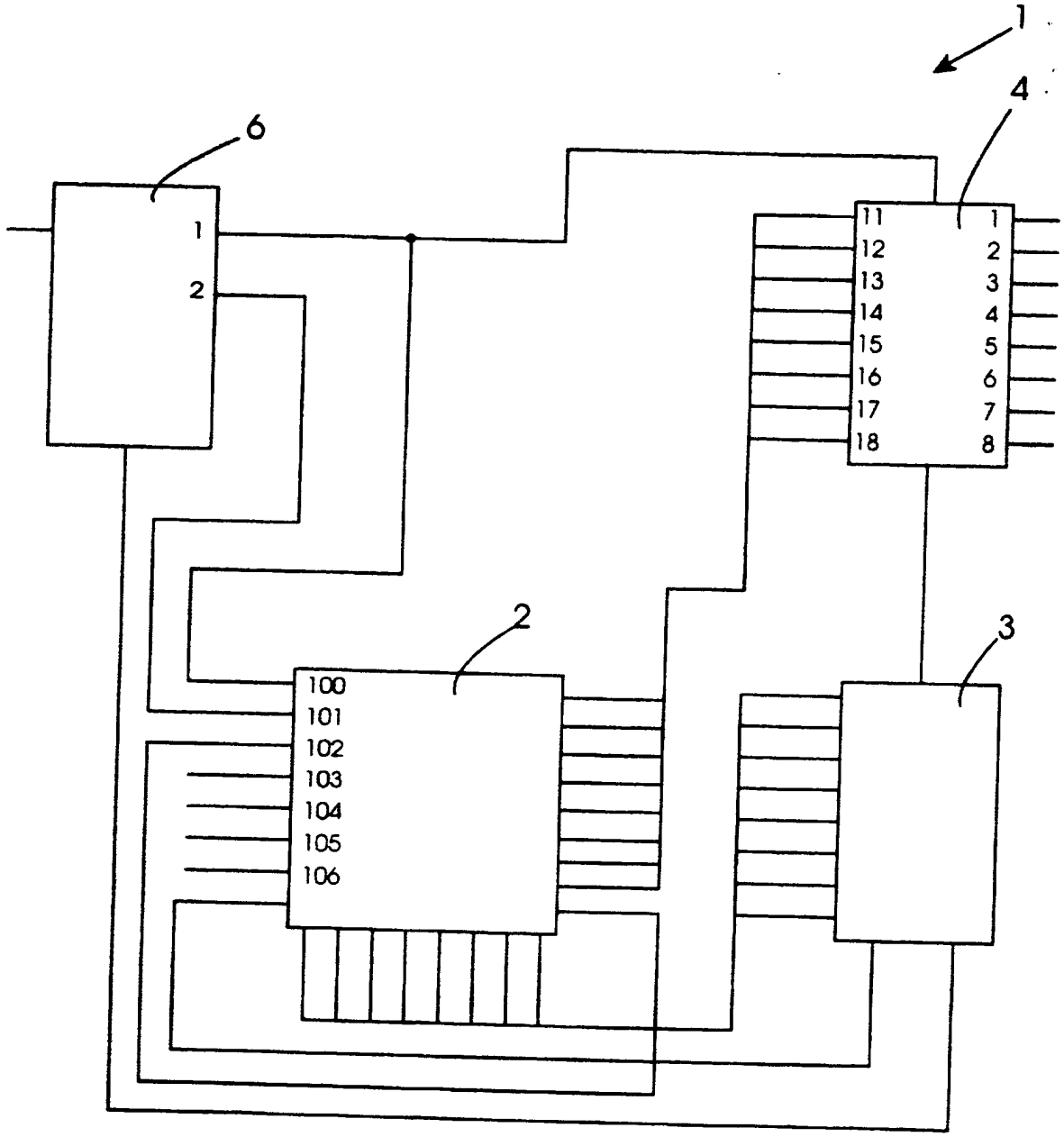

Fig. 1

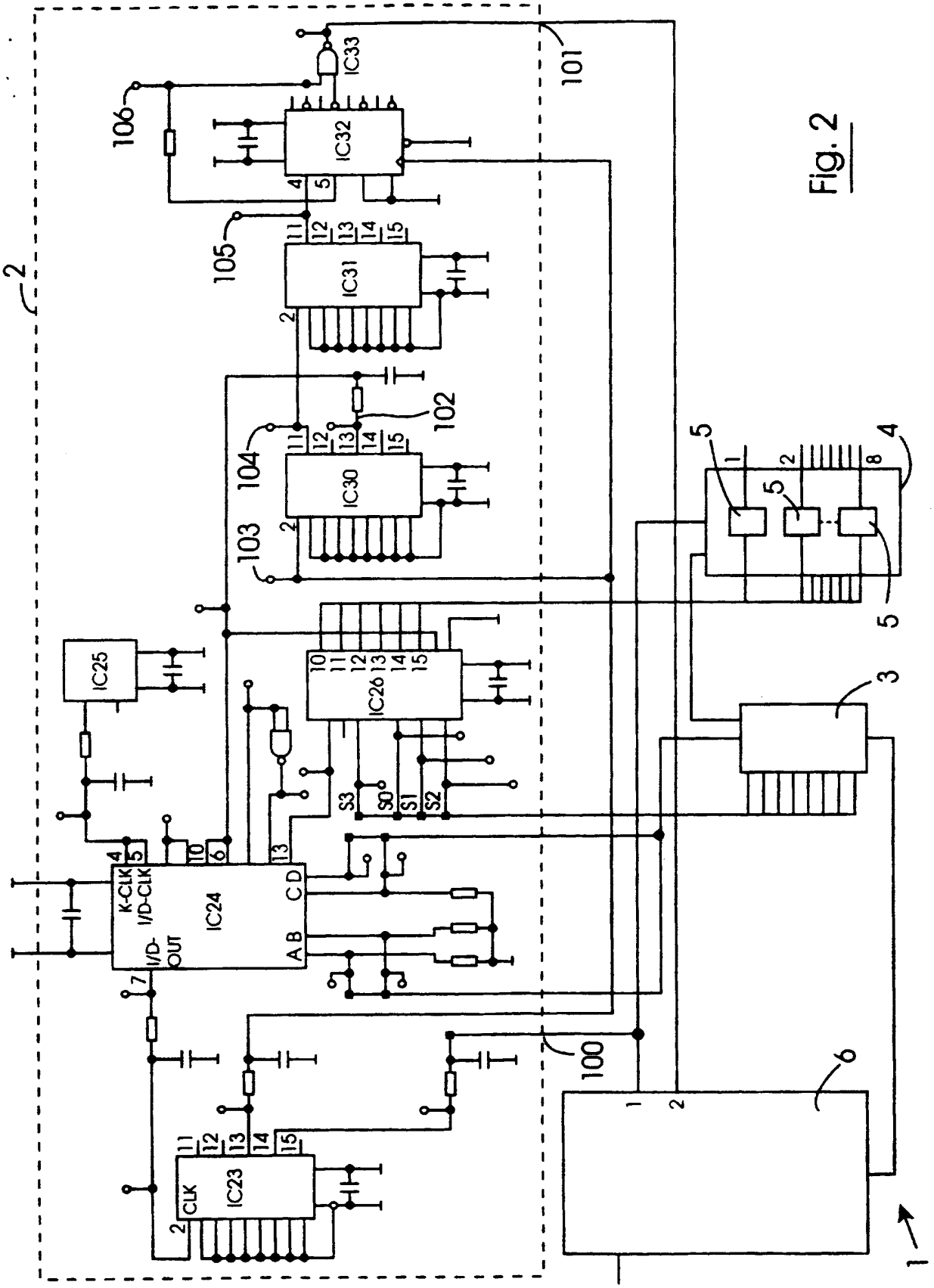

Fig. 2

"A synchronising circuit for a PBX for synchronising a PCM clock signal with basic rate ISDN network signals"

The present invention relates to a synchronising circuit for a private branch exchange (PBX) for providing a synchronised pulse coded modulated (PCM) clock signal synchronised with basic rate ISDN network signals, and in particular, to a synchronising circuit for providing a PCM clock signal for clocking ISDN signals through a digital switch matrix of a communications circuit of the PBX so that the synchronised PCM clock signal is synchronised with basic rate ISDN network signals derived from one of a plurality of ISDN lines interfaced with the PBX. The invention also relates to a method for providing a synchronised PCM clock signal which is synchronised with basic rate ISDN network signals from a selected one of a plurality of ISDN lines. The invention further relates to a PBX comprising synchronising circuit.

It is essential that PCM clock signals generated in the communications circuit of a PBX, including PCM clock signals which are provided for clocking ISDN signals through a digital switch matrix of the communications circuit should be synchronised with basic rate ISDN

network signals which are provided on an ISDN network line. Otherwise, ISDN signals would overflow from buffers within the communications circuit, and would thus be lost.

The present invention is directed towards providing a synchronising circuit which provides a synchronised PCM clock signal which is synchronised with basic rate ISDN network signals, and the invention is also directed towards providing a PBX comprising the synchronising circuit. The invention is further directed towards providing a method for providing a synchronised PCM clock signal which is synchronised with basic rate ISDN network signals.

According to the invention there is provided a synchronised PCM clock signal for a digital switch matrix of a PBX communications circuit synchronised with a basic rate ISDN network signal, the synchronising circuit comprising

an interface means for interfacing a plurality of ISDN lines with the digital switch matrix and for outputting a plurality of corresponding line synchronous clock signals in response to the bit rate of the ISDN signals on the respective corresponding ISDN lines,

a signal generating means for generating a high

frequency clock signal,

a means for deriving and outputting a PCM clock signal from the high frequency clock signal outputted from the signal generating means,

a comparing means for comparing the outputted PCM clock signal from the deriving means with a selected one of the line synchronous clock signals,

a digitally controlled means for altering the outputted PCM clock signal from the deriving means so that the outputted PCM clock signal is synchronised with the selected line synchronous clock signal for providing the synchronised PCM clock signal for clocking the ISDN signals through the digital switch matrix, and

a feedback loop for feeding back the synchronised PCM clock signal to the interface means for facilitating clocking of the ISDN signal through the digital switch matrix of the PBX.

In one embodiment of the invention the means for altering the outputted PCM clock signal from the deriving means comprises an incrementing circuit and a decrementing circuit for selectively adding pulses to or deleting pulses from the outputted PCM clock signal for synchronising the PCM clock signal, the pulses being added to the outputted PCM clock signal being at the frequency of the outputted PCM clock signal.

In another embodiment of the invention the means for altering the outputted PCM clock signal comprises a digitally controlled oscillator having an up/down counter for adding or deleting the pulses.

Preferably, the pulses are added to or deleted from the outputted PCM clock signal by the altering means in response to an error signal derived from the comparing means.

In another embodiment of the invention the comparing means comprises a phase detecting means for detecting the phase of the selected line synchronous clock signal and the phase of the outputted PCM clock signal, the error signal being derived from the phase detecting means.

Preferably, the deriving means, the comparing means and the digitally controlled altering means are provided by a digital phase locked loop circuit. Advantageously, the digital phase locked loop circuit is implemented in the form of an integrated circuit chip.

Advantageously, dividing means is provided for dividing the synchronised outputted PCM clock signal for providing the synchronised PCM clock signal at a desired frequency for clocking the ISDN signals through

the digital switch matrix of the PBX. Preferably, the digital dividing means divides the synchronised outputted PCM clock signal for providing a synchronised PCM clock signal at a frequency substantially similar to the frequency of the selected line synchronous clock signal for feeding to the comparing means for comparison with the select line synchronous clock signal. Advantageously, the digital dividing means divides the synchronised outputted PCM clock signal for providing a frame synchronous clock signal for clocking the ISDN signals through the digital switch matrix of the PBX.

In another embodiment of the invention a selecting means is provided for selecting one of the line synchronising clock signal for feeding to the comparing means, the selecting means being responsive to ISDN signals on the respective ISDN lines.

In a further embodiment of the invention a deselecting means is provided for deselecting the altering means so that the outputted PCM clock signal outputted by the deriving means bypasses the altering means for providing a PCM clock signal which is not synchronised.

Additionally, the invention provides a PBX comprising a communications circuit having a digital switch matrix,

and comprising the synchronising circuit according to the invention for providing a synchronised PCM clock signal synchronised with basic rate ISDN network signals for clocking ISDN signals from an ISDN line through the digital switch matrix.

Further the invention provides a method for providing a synchronised PCM clock signal synchronised with basic rate ISDN network signals from one of a plurality of ISDN lines for clocking ISDN signals through a digital switch matrix of a communications circuit of a PBX, the method comprising the steps of

interfacing a plurality of ISDN lines with the digital switch matrix and providing a plurality of line synchronous clock signals corresponding to ISDN signals on the respective ISDN lines, each line synchronous clock signal being responsive to the bit rate of the ISDN signal on the corresponding ISDN line,

generating a high frequency clock signal,

deriving a PCM clock signal from the high frequency clock signal, and outputting the derived PCM clock signal,

comparing the outputted PCM clock signal with a selected one of the line synchronous clock signals,

altering the outputted PCM clock signal by a digitally controlled means so that the PCM clock signal is synchronised with the selected line synchronous

clock signal for providing the synchronised PCM clock signal for clocking the ISDN signals through the digital switch matrix, and

feeding back the synchronised PCM clock signal to the interface means for facilitating clocking of the ISDN signals through the digital switch matrix of the PBX.

The invention will be more clearly understood from the following description of a preferred embodiment thereof which is given by way of example only with reference to the accompanying drawings, in which:

Fig. 1 is a block representation of a communications circuit of a PBX according to the invention, and

Fig. 2 is a circuit diagram of a synchronising circuit also according to the invention of the communications circuit of Fig. 1.

Referring to the drawings and initially to Fig. 1 there is illustrated a communications circuit of a PBX according to the invention which is indicated generally by the reference numeral 1 for receiving a plurality of ISDN lines, in this case eight ISDN lines for switching through to a plurality of extension lines. A

synchronising circuit 2 also according to the invention in the communications circuit 1 provides a plurality of synchronised PCM signals of different frequencies for the communications circuit 1 as will be described below, and which are synchronised with the basic rate ISDN signals on a selected one of the ISDN lines. The communications circuit 1 comprises a control means, namely, a control circuit which is illustrated in block representation by the block 3. The control circuit 3 comprises a central processing unit (not shown), amongst other components (none of which are shown) for controlling the communications circuit and other aspects of the PBX which will be well known to those skilled in the art.

An interface means which comprises an interface circuit which is illustrated in block representation by the block 4 interfaces the communications circuit 1 with the eight ISDN lines. The interface circuit 4 operates under the control of the control circuit 3. The eight ISDN lines are received by the interface circuit 4 on inputs 1 to 8 of the circuit 4. In this embodiment of the invention the interface circuit 4 comprises eight layer one integrated circuit chips 5, one being provided for each ISDN line. Three of the layer one integrated circuit chips 5 are illustrated in Fig. 2. The layer one integrated circuit chips 5 output

corresponding line synchronous clock signals which are outputted from the interface circuit 4 on outputs 11 to 18. The line synchronous clock signal outputted by each layer one integrated circuit chip 5 is derived from, and in phase with the bit rate of the ISDN signal appearing on the ISDN line to which the layer one integrated chip 5 is connected. In this embodiment of the invention the line synchronous clock signals are at a frequency of 512KHz and are used for maintaining the synchronised PCM clock signals synchronised with the basic rate ISDN signals.

A digital switch matrix which is illustrated in block representation by the block 6 switches calls from the ISDN lines through to the appropriate extension. The digital switch matrix 6 is operated under the control of the control circuit 3.

The synchronising circuit 2 is operated under the control of the control circuit 3, and provides the synchronised PCM clock signals on outputs 100, 101, 102, 103, 104, 105 and 106 at different frequencies as will be described below, which are synchronised with the basic rate ISDN signal on a selected one of the ISDN lines. The synchronised PCM clock signal on the output 100 is at a frequency of 4.096MHz and is applied to an input 1 of the digital switch matrix 6 for

clocking ISDN signals through the digital switch matrix 6. The synchronised PCM clock signal on the output 100 of the synchronising circuit 2 is also fed back to the layer one integrated circuit chips 5 of the interface circuit 4 for closing the control loop. The synchronised PCM clock signal on the output 101 is a frame synchronisation clock signal, and is at a frequency of 8KHz. The frame synchronisation clock signal is applied to an input 2 of the digital switch matrix 6 also for clocking the ISDN signals through the digital switch matrix 6. The synchronised PCM clock signal on the output 102 is at a frequency of 512KHz which is similar to the frequency of the line synchronous clock signals outputted by the interface circuit 3, and is fed back into the synchronising circuit 2 for comparison with a selected one of the line synchronous clock signals for facilitating further correction of the synchronised PCM clock signal. The PCM clock signals of other frequencies on the outputs 103 to 106 are provided for other functions in the communications circuit 1.

Referring now to Fig. 2 the synchronising circuit 2 according to the invention will now be described in detail. The synchronising circuit 2 comprises a digital phase locked loop integrated circuit IC 24 which outputs a synchronised PCM clock signal at a

frequency of 8.192MHz on its I/D_OUT pin 7. The PCM clock signal on pin 7 is derived from a high frequency clock signal generating means, namely, a crystal oscillator IC 25 which applies a clock signal at a frequency of 16.384MHz to the K_CLK and I/D_CLK pins 4 and 5, respectively, of the digital phase locked loop circuit IC 24. The synchronised PCM clock signal at approximately 8.192MHz is fed from the pin 7 of the digital phase locked loop circuit IC 24 to a dividing means, namely, a digital counter IC 23. The counter IC 23 divides the synchronised clock signal at 8.192MHz which is received on its input clock pin 2, and outputs a number of clock signals at different frequencies on its output pins 11 to 15. The output clock signal appearing on pin 14 is at a frequency of 4.096MHz in other words half the input frequency of 8.192MHz, and this signal appearing on pin 14 provides the synchronised PCM clock signal which is outputted on the output 100 of the synchronising circuit 2, and which is applied to the input 1 of the digital switch matrix 6 for clocking the ISDN signals through the digital switch matrix 6. The clock signal appearing on the output pin 13 of the counter IC 23 is at a frequency of approximately 2.048MHz, in other words a quarter of the synchronised PCM clock signal of 8.192MHz which is applied to the input pin 2 of the counter IC 23. This clock signal which appears on pin 13 of the counter

IC 23 is further divided in digital counters IC 30 and IC 31, and in a flip-flop IC 32. An NAND gate IC 33 receives the divided clock signal from the flip-flop IC 32 and outputs the frame synchronisation signal at the frequency of 8KHz which is applied to the input 2 of the digital switch matrix 6. The clock signals which appear on the outputs 103, 104, 105 and 106 of the synchronising circuit 2 for other functions within the PBX are provided on terminals 103, 104, 105 and 106 as can be seen in Fig. 2. The signal appearing on the terminal 103 is derived from the pin 13 of the counter IC 23, the signals on the terminals 104 and 105 are derived from the pins 11 of the counters IC 30 and IC 31, respectively, while the signal on the terminal 106 is derived from the pin 5 of the flip-flop IC 32.

The signal at the frequency of 512KHz on the output 102 of the synchronising circuit 2, in other words the signal at a frequency which is similar to the frequency of the line synchronous clock signals is derived from an output pin 13 of the counter IC 30. The signal on the output pin 13 of the counter IC 30 is in phase with the synchronised PCM coded clock signal which is provided on pin 7 of the digital phase locked loop circuit IC 24 and is fed to input pins 6 and 10 of the digital phase locked loop circuit IC 24 for comparison with the selected one of the line synchronous clock

signals.

A selecting means for selecting one of the line synchronous clock signals from the layer one integrated circuit chips 4 comprises a multiplexer IC 26. The line synchronous clock signals are applied to pins 10 to 15 of the multiplexer IC 26, and a select signal from the control circuit 3 applied to pins S0, S1, S2 and S3 of the multiplexer IC 26 selects the line synchronous clock signal which is to be compared in the phase locked loop circuit IC 24 with the signal from the pin 13 of the counter IC 30. The selected line synchronous clock signal is fed from the multiplexer IC 26 to pin 13 of the digital phase locked loop circuit IC 24, and a comparing means, which is provided by a phase detecting means, namely, phase detectors in the digital phase locked loop circuit IC 24 compares the selected line synchronous clock signal with the signal from the pin 13 of the counter IC 30. If the two signals are not in phase the phase detectors provide an error signal. The error signal is used by an up/down counter of a digitally controlled oscillator in the digital phase locked loop circuit IC 24 for altering the PCM clock signal appearing on the output pin 7 of the digital phase locked loop circuit IC 24 so that it is brought into phase and frequency locked with the selected line synchronous clock signal from the

multiplexer IC 26. This is achieved by an increment/decrement circuit which is provided in the digital phase locked loop circuit IC 24 which adds single pulses at a frequency of 8.192MHz to, or deletes single pulses from the signal which is appearing on pin 7 of the digital phase locked loop circuit IC 24 so that the PCM clock signal appearing on pin 7 is pushed into phase and frequency locked with the selected line synchronous clock signal. In this way the PCM clock signal which is provided at approximately 4.096MHz on the output pin 14 of the counter IC 23 is retained in synchronisation with the basic rate ISDN signal which is being clocked through the digital switch matrix 6. Thus, there is no danger of bits in the ISDN signal which is being received on one of the ISDN lines being lost as it is being clocked through the digital switch matrix 6. Additionally, the frame synchronisation signal of 8KHz which is provided by the NAND gate IC 33 on the output 101 of the synchronising circuit 2 is also retained in synchronisation with the basic grade ISDN network signal.

The synchronised PCM clock signal at approximately 4.096MHz is also fed from the output pin 14 of the digital counter IC 23 to the layer one integrated circuit 4 of the interface circuit 3, thus closing the digital phase locked loop. Depending on the type of

layer one integrated circuits which are used, it may be necessary, to adapt the frame synchronous pulse and relative phase of the frame synchronous pulse and the relative phase of the 4.096MHz clock signal and the frame synchronous pulse. This is carried out in the digital switch matrix 6.

A deselect means is provided for deselecting the digital phase locked loop circuit IC 24 so that the output appearing on the pin 7 of the digital phase locked loop circuit IC 24 is derived directly from the crystal oscillator IC 25. In this way, the PCM signal outputted on the pin 7 of the digital phase locked loop circuit IC 24 is not synchronised with an ISDN line. The digital phase locked loop circuit IC 24 is deselected by a signal from the control circuit 2 which is applied to the pins A, B, C and D of the digital phase locked loop circuit IC 24. The communications circuit 1 would be operated with the digital locked loop circuit deselected for receiving signals from an analog public network exchange line.

The invention is not limited to the embodiment hereinbefore described which may be varied in construction and detail.

CLAIMS

1. A synchronising circuit for providing a synchronised PCM clock signal for a digital switch matrix of a PBX communications circuit synchronised with a basic rate ISDN network signal, the synchronising circuit comprising

an interface means for interfacing a plurality of ISDN lines with the digital switch matrix and for outputting a plurality of corresponding line synchronous clock signals in response to the bit rate of the ISDN signals on the respective corresponding ISDN lines,

a signal generating means for generating a high frequency clock signal,

a means for deriving and outputting a PCM clock signal from the high frequency clock signal outputted from the signal generating means,

a comparing means for comparing the outputted PCM clock signal from the deriving means with a selected one of the line synchronous clock signals,

a digitally controlled means for altering the outputted PCM clock signal from the deriving means so that the outputted PCM clock signal is synchronised with the selected line synchronous clock signal for providing the synchronised PCM clock signal for clocking the ISDN signals through the digital switch matrix, and

a feedback loop for feeding back the synchronised PCM clock signal to the interface means for facilitating clocking of the ISDN signal through the digital switch matrix of the PBX.

2. A synchronising circuit as claimed in Claim 1 in which the means for altering the outputted PCM clock signal from the deriving means comprises an incrementing circuit and a decrementing circuit for selectively adding pulses to or deleting pulses from the outputted PCM clock signal for synchronising the PCM clock signal, the pulses being added to the outputted PCM clock signal being at the frequency of the outputted PCM clock signal.

3. A synchronising circuit as claimed in claim 2 in which the means for altering the outputted PCM clock signal comprises a digitally controlled oscillator having an up/down counter for adding or deleting the pulses.

4. A synchronising circuit as claimed in Claims 2 or 3 in which the pulses are added to or deleted from the outputted PCM clock signal by the altering means in response to an error signal derived from the comparing means.

5. A synchronising circuit as claimed in Claim 4 in which the comparing means comprises a phase detecting means for detecting the phase of the selected line synchronous clock signal and the phase of the outputted PCM clock signal, the error signal being derived from the phase detecting means.

6. A synchronising circuit as claimed in any preceding claim in which the deriving means, the comparing means and the digitally controlled altering means are provided by a digital phase locked loop circuit.

7. A synchronising circuit as claimed in Claim 6 in which the digital phase locked loop circuit is implemented in the form of an integrated circuit chip.

8. A synchronising circuit as claimed in any preceding claims in which a digital dividing means is provided for dividing the synchronised outputted PCM clock signal for providing the synchronised PCM clock signal at a desired frequency for clocking the ISDN signals through the digital switch matrix of the PBX.

9. A synchronising circuit as claimed in Claim 8 in which the digital dividing means divides the synchronised outputted PCM clock signal for providing a

synchronised PCM clock signal at a frequency substantially similar to the frequency of the selected line synchronous clock signal for feeding to the comparing means for comparison with the select line synchronous clock signal.

10. A synchronising circuit as claimed in Claim 8 or 9 in which the digital dividing means divides the synchronised outputted PCM clock signal for providing a frame synchronous clock signal for clocking the ISDN signals through the digital switch matrix of the PBX.

11. A synchronising circuit as claimed in any preceding claim in which a selecting means is provided for selecting one of the line synchronising clock signal for feeding to the comparing means, the selecting means being responsive to ISDN signals on the respective ISDN lines.

12. A synchronising circuit as claimed in any preceding claim in which a deselecting means is provided for deselecting the altering means so that the outputted PCM clock signal outputted by the deriving means bypasses the altering means for providing a PCM clock signal which is not synchronised.

13. A synchronising circuit substantially as

described herein with reference to and as illustrated in the accompanying drawing.

14. A PBX comprising a communications circuit having a digital switch matrix, and comprising the synchronising circuit as claimed in any preceding claim for providing a synchronised PCM clock signal synchronised with basic rate ISDN network signals for clocking ISDN signals from an ISDN line through the digital switch matrix.

15. A PBX substantially as described herein with reference to and as illustrated in the accompanying drawings.

16. A method for providing a synchronised PCM clock signal synchronised with basic rate ISDN network signals from one of a plurality of ISDN lines for clocking ISDN signals through a digital switch matrix of a communications circuit of a PBX, the method comprising the steps of

interfacing a plurality of ISDN lines with the digital switch matrix and providing a plurality of line synchronous clock signals corresponding to ISDN signals on the respective ISDN lines, each line synchronous clock signal being responsive to the bit rate of the ISDN signal on the corresponding ISDN line,

generating a high frequency clock signal,

deriving a PCM clock signal from the high frequency clock signal, and outputting the derived PCM clock signal,

comparing the outputted PCM clock signal with a selected one of the line synchronous clock signals,

altering the outputted PCM clock signal by a digitally controlled means so that the PCM clock signal is synchronised with the selected line synchronous clock signal for providing the synchronised PCM clock signal for clocking the ISDN signals through the digital switch matrix, and

feeding back the synchronised PCM clock signal to the interface means for facilitating clocking of the ISDN signals through the digital switch matrix of the PBX.

17. A method for providing a synchronised PCM clock signal synchronised with basic rate ISDN network signals from one of a plurality of ISDN lines for clocking ISDN signals through a digital switch matrix of a communications circuit of a PBX, the method being substantially as described herein with reference to and as illustrated in the accompanying drawings.

The Patent Office

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Claims searched: 1-17

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Date of search: 18 March 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H4K(KTA)

Int Cl (Ed.6): H04J 3/06 H04Q 11/04

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2257603 A	(GENERAL ELECTRIC) see Fig 2	-
A	GB 2220327 A	(TOSHIBA) see Fig 4	-
A	US 5136617	(AT&T BELL LABORATORIES) see Fig 1	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.